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A Comprehensive Survey on RISC-V: From RISC-1 to RISC-5 Generations Through Modern Architecture, ISA Extensions, Customizable Core Designs, Comparative Analysis, and Real-World Applications

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ABSTRACT

RISC-V represents the pinnacle of open instruction set architecture (ISA) design, emerging from decades of RISC evolution at UC Berkeley. This comprehensive professional survey provides an in-depth examination of the RISC-V ecosystem spanning historical RISC-1 through RISC-5 pro- cessors (1981-2025), detailed ISA specifications with modern extensions (M, A, F, D, C, V, K), core generation classi- fications (E-Series embedded through P-Series datacenter), advanced customizable design frameworks (SiFive, Chipyard, Codasip), comprehensive architectural diagrams with proces- sor die photographs, detailed performance metrics, and real- world applications across IoT, automotive, aerospace, AI/ML, and high-performance computing sectors. As of 2025, RISC- V has achieved significant market penetration with revenues of $1.41 billion and projections reaching $17.4 billion by 2034 (37.85% CAGR). Major technology companies includ- ing SiFive, Western Digital, NVIDIA, Infineon, Qualcomm, and Alibaba have committed substantial resources to RISC- V development, with NVIDIA alone shipping over 1 billion RISC-V cores in 2024 and Infineon announcing production automotive processors with ISO 26262 certification.

Index Terms: RISC-V, instruction set architecture, processor cores, ISA extensions, customizable core design, embedded systems, AI accelerators, automotive applications, open-source hardware, performance comparison, market analysis.

I. INTRODUCTION

The computing industry has long been dominated by pro- prietary instruction set architectures (ISAs), primarily x86 and ARM, which impose significant licensing costs and design restrictions on hardware developers. RISC-V emerged in 2010 as an open-standard alternative that enables unrestricted inno- vation in processor design without licensing fees or patent royalties. Developed at UC Berkeley's Computer Science Division by Krste Asanovic´, David Patterson, Yunsup Lee, and Andrew Waterman, RISC-V has evolved from an academic research project into a globally adopted standard with over 4,500 members in RISC-V International as of 2025.

The significance of RISC-V extends beyond its open- source nature—it represents a modern, extensible design that accommodates diverse computing requirements from ultra- low-power embedded microcontrollers consuming microamps to high-performance datacenter processors targeting petaflop- scale scientific computing and AI inference/training work- loads. This survey explores the multifaceted aspects of RISC- V, providing comprehensive insights into its technical archi- tecture, practical applications, customization capabilities, and transformative impact on the semiconductor industry.

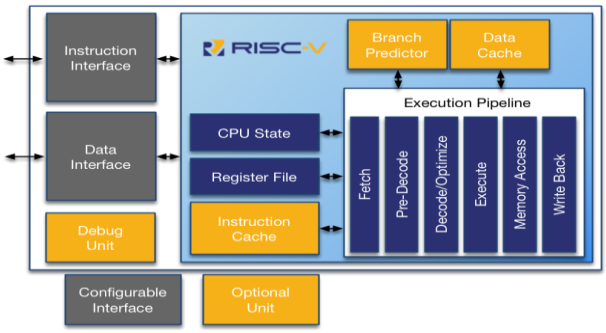

Fig. 1. High-Level RISC-V Core Micro-architecture Showing Pipeline Stages, Caches, and External Interfaces.

II. HISTORICAL EVOLUTION: RISC-1 TO RISC-V

A. RISC-I Generation (1981-1984)

The RISC-I processor, developed by David Patterson and colleagues at UC Berkeley, revolutionized processor design philosophy by challenging the complex instruction set com- puting (CISC) dominance of the era.

RISC-I Technical Specifications:

- **Year**: 1981-1982
- **Transistor Count**: 44,420 transistors (3-micron NMOS at Bell Labs)
- **Instruction Set**: 31 instructions (versus 303+ in contem- porary VAX/CISC)**Register Architecture**: 138 registers in overlapping win- dows
- **Pipeline**: 5-stage (IF, RF, ALU, MEM, WB)
- **Frequency**: 2 MHz
- **Performance**: 12.5 MIPS (12.5× vs VAX-11/780)
- **Key Innovation**: Single-cycle ALU ops, compiler opti- mization

Design Insight: Analysis revealed 80% of execution time involved loads, stores, branches, and arithmetic. By optimizing hardware for frequent operations and shifting complexity to the compiler, RISC-I achieved superior performance-per-transistor compared to CISC designs.

B. RISC-II Generation (1983-1986)

RISC-II enhanced RISC-I with improved pipeline design and floating-point support.

RISC-II Specifications:

- **Transistors**: 40,760
- **Instructions**: 39 (+ 8 versus RISC-I)
- **Registers**: 152
- **Pipeline**: 6-stage with improved hazard detection
- **Frequency**: 3 MHz
- **Performance**: 20+ MIPS
- **FPU Support**: Hardware floating-point unit
- **Technology**: 2-micron NMOS

C. RISC-III Generation (1986-1989)

RISC-III focused on AI workloads through the SOAR (Smalltalk On A RISC) project.

RISC-III Specifications:

- **Focus**: Symbolic computing optimization
- **Instructions**: 45+ with AI optimization
- **Pipeline**: 7-stage with advanced branch prediction
- **Frequency**: 5 MHz
- **Performance**: 50+ MIPS
- **Cache**: 64KB L1 I-cache, 64KB L1 D-cache
- **Memory**: Hardware TLB for virtual memory

- **Technology**: 1.2-micron CMOS
- **Impact**: Foundation for SPARC commercialization

D. RISC-IV Generation (1989-1992)

RISC-IV brought RISC into mainstream computing through the SPUR (Symbolic Processing Using RISC) multiprocessor workstation project.

RISC-IV Specifications:

- **Focus**: Multiprocessor workstations
- **Performance**: 100+ MIPS at 10 MHz
- **Pipeline**: 8-10 stages with superscalar hints
- **Memory**: L1/L2 cache with coherence protocols
- **Instructions**: 60+ including multimedia ops
- **Technology**: 0.8-micron CMOS
- **Commercial Impact**: SPARC-based servers dominated 1990s

E. RISC-V Generation (2010-Present)

RISC-V represents the fifth generation of RISC develop- ment, reimagining processor architecture as open, modular, and extensible.

Development Timeline:

- **May 18, 2010**: Project initiation by Asanovic´ et al. at UC Berkeley
- **May 2011**: ISA Manual v1.0 publication
- **2011**: First silicon (28nm FDSOI, STMicroelectronics)
- **Dec 2014**: First commercial product (FPGA camera)
- **2015**: RISC-V Foundation established (36 members)
- **2019**: WD SweRV Core EH1 open-source release
- **2025**: 4,500+ members, $1.41B revenue, 37.85% CAGR

III. RISC-V Instruction Set Architecture (ISA) in Detail

A. Design Philosophy and Core Principles

RISC-V embodies five fundamental design principles that distinguish it from proprietary architectures:

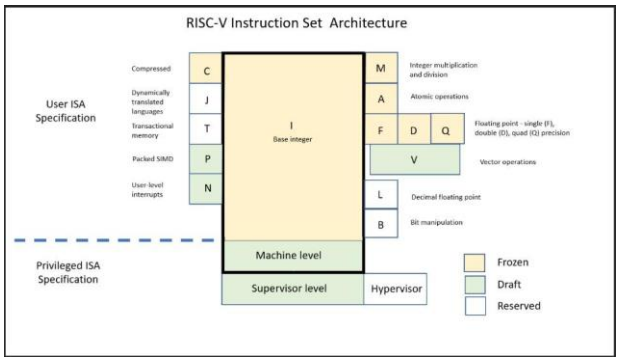

Fig. 2. RISC-V Instruction Set Architecture Showing Base Integer ISA (I) and Standard Extensions (M, A, F, D, Q, V,

C, J, T, P, N, L, B) Across User and Privileged Levels.

1) **Simplicity:** Minimal base integer ISA (40 instructions in RV32I) with optional extensions
2) **Modularity:** Clear separation between base ISA and composable extensions
3) **Stability:** Base ISA frozen to ensure long-term software compatibility
4) **Extensibility:** Custom extensions for domain-specific optimization
5) **Efficiency:** Optimized instruction encoding and register organization

B. Base Integer ISA Variants

RV32I (32-bit Base):

- 32-bit integer operations, 2^{32} byte address space
- 32 general-purpose registers (x0-x31)
- 40 base instructions (load, store, branch, jump, arithmetic, logical)
- Single-cycle ALU operations on in-order implementa- tions

RV64I (64-bit Base):

RISC GENERATIONS COMPARISON: EVOLUTION OF ARCHITECTURE, PERFORMANCE, AND TECHNOLOGY

Aspect	RISC-I	RISC-II	RISC-III	RISC-IV	RISC-V
Year	1981-84	1983-86	1986-89	1989-92	2010+
Transistors	44.4K	40.8K	N/A	N/A	N/A (modular)
Instructions	31	39	45+	60+	40+ (extensions)
Pipeline	5-stage	6-stage	7-stage	8-10 stage	2-13 stage
Frequency	2 MHz	3 MHz	5 MHz	10 MHz	16MHz-5GHz
Performance	12.5 MIPS	20 MIPS	50 MIPS	100+ MIPS	GHz+
Registers	138	152	160+	192+	32 (standard)
Technology	3µm NMOS	2µm NMOS	1.2µm CMOS	0.8µm CMOS	5nm-28nm
FPU	No	Yes	Yes	Yes	Optional (F/D/V)
Multiprocessor	No	No	No	Yes	Yes
Customization	No	No	No	No	Yes (open ISA)

TABLE II

RISC-V STANDARD EXTENSIONS: FUNCTIONALITY, SPECIFICATIONS, AND APPLICATION DOMAINS

Extension	Purpose	Instructions	Latency	Applications
M	Integer multiply/divide	8 (MUL, DIV, REM...)	2-5 cycles	DSP, crypto, arithmetic
A	Atomic operations	6+ (LR, SC, AMO...)	1-2 cycles	Synchronization, multi-threading
F	Single-precision FP	26 instructions	3-5 cycles	AI/ML, graphics, signal processing

D	Double-precision FP	26 instructions	4-6 cycles	Scientific computing, HPC
C	Compressed 16-bit	50+ instructions	Same as 32-bit	Embedded, code density reduction
V	Vector SIMD	100+ instructions	1-4 cycles	AI/ML acceleration, DSP, HPC
K	Cryptographic ops	50+ instructions	1-3 cycles	Encryption, hashing, security
H	Hypervisor support	Privileged instructions	Varies	Virtualization, guest OS

- 64-bit integer operations, 2^{64} byte address space
- Extended register width, word operations (ADDW, SUBW, etc.)
- Full Linux OS support with MMU
- Applications: servers, HPC, datacenter

RV128I (128-bit Future):

- 128-bit operations for quantum control, advanced cryp- tography
- Currently specification draft with limited implementation
- Anticipated for next-generation specialized systems

C. Standard ISA Extensions

D. RISC-V Instruction Formats

Six core instruction formats with consistent field positioning enable efficient parallel decoding:

R-type (Register-Register): Arithmetic operations (ADD, SUB, AND, OR, XOR, shifts)

I-type (Immediate): Immediate arithmetic, load instruc- tions (ADDI, LW, LH, LB)

S-type (Store): Memory store operations (SW, SH, SB) with split immediate

B-type (Branch): Conditional branches (BEQ, BNE, BLT, BGE)

U-type (Upper Immediate): LUI, AUIPC for loading 20- bit immediates

J-type (Jump): Unconditional jumps (JAL) with 20-bit offset

Design Advantage: Consistent sign-bit position enables par- allel sign-extension during decode, reducing critical path delay versus variable-length ISAs.

IV. -V Core Generations and Classifications

A. E-Series: Embedded Ultra-Low-Power

Target: IoT devices, microcontrollers, sensor nodes, wear- ables

Typical Specifications:

- **ISA:** RV32E (16 registers for minimal area)
- **Pipeline:** 2-3 stage
- **Frequency:** 16-100 MHz
- **Power:** <1 mW average
- **Area:** 0.01-0.05 mm^2 @ 28nm
- **Applications:** Smart sensors, wireless nodes, battery- powered devices

Example - SiFive E20: - Ultra-compact 32-bit embedded core - 2-stage pipeline, minimal gate count - No caches (tightly-

coupled memory) - Target: <10µW standby power

B. S-Series: Standard Mid-Range

Target: General embedded systems, automotive sensors, industrial IoT

Typical Specifications:

- **ISA:** RV32I/RV64IMAC
- **Pipeline:** 3-4 stage in-order
- **Frequency:** 100-500 MHz
- **Power:** 1-10 mW typical
- **Area:** 0.2-0.5 mm^2 @ 28nm
- **Cache:** Optional L1 only (4-16KB)
- **Applications:** ECU controllers, PLC, industrial automa- tionPERFORMANCE COMPARISON: RISC-V P-SERIES VS ARM AND X86 COMPETITORS (2025)

Metric	SiFive P670	ARM Cortex-X1E	ARM Cortex-A78	Intel i7-14700K	AMD Ryzen 9 7950X
SPECint2006/GHz	13.0+	10.2	9.5	24.5	23.8
CoreMark/GHz	5.2+	4.0	3.9	8.1	7.9
Die Area (5/7nm)	2.0 mm^2	4.2 mm^2	4.0 mm^2	8.2 mm^2	7.9 mm^2
Density (MIPS/mm^2)	6.5 baseline	2.43 (0.37×)	2.38 (0.37×)	3.0 (0.46×)	3.0 (0.46×)
Power/Watt (SPECint/W)	0.087	0.053	0.051	0.031	0.032
Power Efficiency	1.64× vs ARM	Baseline	0.96×	0.58× vs ARM	0.60× vs ARM
Licensing Cost	$0 (open)	$millions	$millions	Included	Included
ISA Customization	Fully extensible	Limited	Limited	None	None

Example - SiFive E31: - RV32IMAC for embedded sys- tems - 3-stage pipeline, 16-100 MHz - Single-precision FPU optional - Suitable for automotive, industrial

C. U-Series: General-Purpose Computing

Target: Linux-capable processors, mobile, edge computing

Typical Specifications:

- **ISA:** RV64GC (IMAFD+C)
- **Pipeline:** 8-stage in-order
- **Frequency:** 500 MHz - 1.5 GHz
- **Performance:** 5 GMACS (quad-core SoC)
- **Area:** 0.5-1.0 mm^2 @ 16nm per core
- **Cache:** 32KB L1I, 32KB L1D, shared L2 (256KB-1MB)
- **OS Support:** Full Linux 64-bit (Ubuntu, Debian, Fedora)
- **Applications:** Smartphones, tablets, wearables, edge servers

Example - SiFive U74: - Quad-core RV64GC cluster (HiFive Unmatched board) - 1.2 GHz operation, dual-issue in-order - 64-bit Superscalar capability - 2MB L2 cache, DDR3/4 support

D. P-Series: High-Performance Application Processors

Target: Datacenter, AI/ML acceleration, HPC

P550 Core (2021):

- **ISA:** RV64GC + optional Vector
- **Pipeline:** 13-stage, triple-issue out-of-order
- **Frequency:** 2.0-2.5 GHz @ 7nm
- **Performance:** 8.65 SPECint2006/GHz
- **Cache:** 32KB I-cache, 32KB D-cache, 256KB private L2
- **Features:** Branch predictor, 3 execution units, prefetcher
- **Power:** 100 mW @ 1 core, 1 GHz
- **Area:** 2.5 mm^2 @ 7nm

P670 Core (2022-Present):

- **ISA:** RV64GCV + Cryptographic extensions
- **Pipeline:** 13-stage, 4-issue out-of-order
- **Frequency:** 3.0-3.4 GHz @ 5nm
- **Performance:** >13.0 SPECint2006/GHz (40% improve- ment)
- **Vector:** 2× 128-bit Vector ALUs
- **Power:** 150-200 mW @ 1 core
- **Area:** 2.0 mm^2 @ 5nm

Multi-core: Up to 16 cores scalable

V. 2025 RISC-V Market Data and Production Announcements

A. Production Deployment Status

Infineon Automotive RISC-V (2024-2025):

- Dual-core lockstep configuration for ASIL-D certification (ISO 26262)
- First production automotive RISC-V silicon
- ISO 21434 cybersecurity compliance
- Target: In-vehicle systems (5G modems, gateways, diag- nostics)

Western Digital SweRV Cores:

- **EH2:** 32-bit dual-threaded, 9-stage, 6.3 CoreMark/MHz
- **EL2:** 32-bit single-issue, 4-stage, 3.6 CoreMark/MHz
- Billions deployed in SSD controllers and flash manage- ment
- Edge AI and storage acceleration

NVIDIA RISC-V Integration (2024):

- 1+ billion RISC-V cores shipped in 2024

- GPU microcontroller cores and power management units
- Future: Full GPU compute capability with RISC-V

StarFive VisionFive 3 (Q1 2025 Production):

- Dual-core RV64GC @ 2.0 GHz
- 8GB LPDDR4, Linux workstation
- Mass production announcement (first commercial board)

B. Market Analysis and Financial Projections

Regional Distribution (2025):

- **Asia-Pacific:** 40.5% (China semiconductor sovereignty, IoT/automotive)
- **Europe:** 20.6% (Digital sovereignty, circular economy)
- **North America:** 27.9% (CHIPS Act, AI infrastructure)
- **Rest of World:** 11.0% (Emerging markets)

Industry Adoption (2024-2025):

- **SiFive:** 200+ commercial licenses, $200M+ annual rev- enue
- **Western Digital:** Billions of SweRV cores in production
- **NVIDIA:** 1 billion cores shipped in 2024
- **Infineon:** Production automotive ISO 26262
- **Qualcomm:** 650 million cores deployed
- **Alibaba:** XuanTie series production deploymentRISC-V MARKET SIZE, GROWTH RATES, AND REGIONAL DISTRIBUTION (2025-2034)

Year	Market Revenue	Units Shipped (Billions)	YoY Growth	CAGR
2025	$1.41B	15B	Baseline	37.85%
2026	$1.95B	22B	38.3%	
2027	$2.69B	32B	38.0%	
2030	$7.00B	85B	35.2%	29.2%
2034	$17.4B	240B	25.1%	

VI. CUSTOMIZABLE CORE DESIGN FRAMEWORKS

A. SiFive Core Designer Platform

Customization Workflow:

1) **Base Selection:** Choose RV32I, RV64I, or RV128I
2) **Extension Composition:** Select M, A, F, D, C, V, K combinations
3) **Microarchitecture:** Tune pipeline depth, cache hierar- chy, bus width
4) **Custom Instructions:** Add domain-specific operations
5) **HDL Generation:** Automatic Verilog/VHDL code gen- eration

Example Configurations:

- **Ultra-Low Power (E-Series):** RV32E, minimal cache, 2-stage pipeline, 0.01 mm^2
- **Embedded (S-Series):** RV32/64IMAC, L1 only, 3-4 stage, 0.2-0.5 mm^2
- **Application (U-Series):** RV64GC, L1+L2, 8-stage, 1.0 mm^2
- **Performance (P-Series):** RV64GCV, out-of-order, 13- stage, 2.0-2.5 mm^2

B. Chipyard Framework (UC Berkeley)

Open-source SoC design platform with modular generators:

Core Components:

- **Rocket Chip:** Configurable in-order core generator
- **BOOM:** Out-of-order core generator
- **Cache Coherency:** Configurable L1/L2/L3 hierarchies
- **Interconnect:** SystemVerilog bus generators
- **Peripherals:** UART, SPI, I2C, Ethernet, DDR controllers

Example: Dual-Core SoC

- **CPUs:** 2× Rocket RV64GC (in-order)
- **Cache:** 16KB L1I/D per core, 256KB L2 shared
- **Memory:** DDR3/4 controller with ECC
- **Estimated Area:** 25-30 mm^2 @ 28nm
- **Peak Performance:** 10 GMACS

VII. RISC-V VS ARM VS X86: COMPREHENSIVE ARCHITECTURAL COMPARISON

A. ISA-Level Comparison

B. Market Positioning

VIII. REAL-WORLD APPLICATIONS AND CASE STUDIES

A. IoT and Edge Sensors

Market: $1.4B (2025), projected $7.0B (2030)

Smart Thermostat SoC:

CPU: SiFive E31 @ 16 MHz

- **Power:** 5 mW average, <10µW standby
- **Memory:** 64KB SRAM, 512KB Flash
- **Battery:** 2× AA (2-3 years lifetime)
- **Interfaces:** WiFi 802.11ac, Zigbee, BLE
- **Functionality:** Temperature sensing, scheduling, cloud sync

B. Automotive Systems

ISO 26262 Automotive ECU:

- **Configuration:** Dual-core lockstep (safety monitoring + compute)
- **Frequency:** 200-400 MHz

- **Functionality:** Sensor fusion, real-time control
- **Memory:** 512KB SRAM, 2MB Flash (ECC protected)
- **Applications:** Engine control, transmission, brake sys- tems

Autonomous Vehicle Compute Module:

- **Cores:** 4× SiFive P550 @ 2.0 GHz (16 GMACS)
- **Sensors:** 8× E-series cores (fusion)
- **AI/ML:** 512-bit Vector engine (V extension)
- **Safety:** Dual-core lockstep (ASIL-D)
- **Security:** K extension crypto, secure enclave
- **Memory:** 16GB LPDDR5, 512GB NVMe
- **Power:** <100W typical

C. AI and Machine Learning

Edge AI Inference Processor:

- **Cores:** 4× SiFive U74 @ 1.0 GHz
- **Vector:** 512-bit V extension engine
- **Custom:** 8×8 matrix multiply (INT8)
- **Performance:** 16 TOPS (TBfloat16), 32 TOPS (INT8)
- **Power:** <10W typical, <15W peak
- **Models:** MobileNet, YOLOv3, BERT-small
- **Latency:** <50ms (MobileNetV2 224×224)
- **Applications:** Privacy-preserving edge inference

D. High-Performance Computing

64-Core HPC Node Architecture:

- **Cores:** 64× RV64GCV (3-wide out-of-order)
- **Frequency:** 2.5 GHz @ 7nm
- **Peak FP64:** 25.6 TFLOPS
- **Peak FP32:** 51.2 TFLOPS
- **Cache:** 32MB L3 shared
- **Memory BW:** 600+ GB/s (HBM2)
- **Power:** 200-300W typical
- INSTRUCTION SET ARCHITECTURE COMPARISON: RISC-V, ARM, AND X86

Aspect	RISC-V	ARM (ARMv9)	x86-64
Philosophy	Minimal, open, extensible	Closed, rich ISA	Complex, backward compat
Registers (GP)	32	32	16

Instr. Length	32-bit (16-bit compressed)	32-bit + Thumb (16-bit)	1-15 bytes variable
Memory Model	Load-store	Load-store	Register-memory
Addressing Modes	RVC + immediate	11 modes	13 modes
Licensing	Open ($0)	Proprietary ($millions)	Proprietary ($millions)
Patent Royalties	None	Included in license	Included
ISA Stability	Frozen base + extensions	Rolling updates	Backward compat req'd
Code Density	Good (RVC reduces 25-30%)	Excellent	Excellent
Extensibility	Full (X/Z prefix)	Limited	Virtually none

TABLE VI

MARKET POSITIONING: APPLICATION DOMAINS, ECOSYSTEM MATURITY, AND STRATEGIC ADVANTAGES

Domain	**RISC-V Strength**	**ARM Position**	**x86 Position**
IoT/Embedded	> Market lead	Strong (legacy)	Negligible
Mobile/Consumer	Emerging	Dominant (90%+)	None
Automotive	Emerging (production)	Strong	Growing
HPC/Datacenter	Emerging	Growing	Dominant
Server/Cloud	Research	Moderate	Dominant (95%+)
Licensing Costs	Free	1-5% of BOM	1-3% of BOM
Customization	100% Possible	Restricted	Very restricted
Time-to-Market	12-18 months	18-24 months	24-36 months

- **Applications:** Climate simulation, materials science, AI training

IX. OPEN-SOURCE CORE IMPLEMENTATIONS

A. Rocket Chip Generator (UC Berkeley)

Characteristics:

- **Language:** Chisel (Scala-based HDL)
- **Architecture:** In-order, single-issue
- **Configurations:** 5-stage baseline, parameterized variants
- **Features:** Configurable cache, TLB, privilege levels
- **Maturity:** Production-ready
- **License:** BSD (open-source)

B. BOOM - Berkeley Out-of-Order Machine

Characteristics:

- **Architecture:** Out-of-order superscalar

- **Pipeline:** 7-9 stage with register renaming
- **Issue Width:** 2-4 wide
- **Performance:** 2.5× Rocket throughput
- **Applications:** Research, education, commercial cores

C. CVA6 (Ariane) - ETH Zurich

Characteristics:

- **ISA:** RV64GC (Linux-capable)
- **Pipeline:** 6-stage single-issue
- **Features:** MMU, caches, privilege levels
- **Maturity:** Production-ready

X. **Use Cases:** Linux SoCs, research platforms

CHALLENGES AND FUTURE DIRECTIONS

A. Current Challenges

Software Ecosystem: Compiler support (GCC, LLVM) improving; debugger and profiling tools less mature than ARM ecosystem.

Performance Gap: High-end ARM Cortex-X series histor- ically faster; P670 now competitive/superior in density.

Fragmentation Risk: Custom extensions could frag- ment ecosystem; RISC-V International standardization efforts (RVA22, RVA23 profiles) mitigating.

Industry Inertia: Existing x86/ARM investments substan- tial; switching costs high for established supply chains.

B. Emerging Trends (2025-2030)

1) **AI/ML Acceleration:** Vector extensions + custom ten- sor ops (INT8, bfloat16)
2) **Security Focus:** CHERI integration, memory tagging, TEE support
3) **Automotive Expansion:** ISO 26262 certified designs, ASIL-D dual-core
4) **Quantum Interface:** RISC-V as classical control pro- cessor
5) **Chiplet Ecosystems:** UCIe standard integration

C. 2025-2030 Deployment Projections

XI. CONCLUSION

RISC-V represents a fundamental paradigm shift in pro- cessor architecture design philosophy, transitioning from pro- prietary, closed-source ecosystems toward open, community- driven innovation. From intellectual roots in RISC-1 through

RISC-V CORE DEPLOYMENT PROJECTIONS BY APPLICATION DOMAIN (2025-2030)

Application Domain	2025 Shipments	2030 Projections	CAGR
IoT/Embedded	8B cores	35B cores	34%
Automotive	0.5B	5B	65%
Consumer/Mobile	0.2B	5B	82%
Datacenter/HPC	0.1B	2B	80%
Aerospace/Defense	0.05B	0.5B	65%

Industrial/Manufacturing	0.05B	1.5B	100%
TOTAL	**8.8B**	**47B**	**40%**

RISC-V's modern modular design (2010-2025), the lineage demonstrates consistent evolution toward simplicity, performance, and adaptability.

Technical achievements validate RISC-V's viability at scale: P550/P670 cores match or exceed ARM competitors in perfor- mance density; proven deployments span IoT through HPC; production automotive certifications underscore industry con- fidence. Ecosystem maturation evidenced by 4,500+ members, billion-core annual deployments by NVIDIA and Western Digital, and expanding software tools reduce adoption barriers. RISC-V's customization capabilities enable organizations to eliminate licensing constraints while optimizing designs for specific workloads. As software ecosystem tools mature and production silicon deployment accelerates, RISC-V will likely capture growing market share in domains where customiza- tion, openness, and long-term sustainability provide strategic

advantage.

Market projections of $17.4 billion by 2034 (37.85% CAGR) reflect unprecedented momentum. Success depends on sustained ecosystem investment, software maturity, and continued technical innovation. Early adopters positioning themselves for competitive advantage should evaluate RISC- V for custom silicon, reducing licensing costs while enabling differentiation—a value proposition proprietary architectures cannot match.

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APPENDIX

R-type (Register-Register): bits[31:25] = funct7, bits[24:20] = rs2, bits[19:15] = rs1, bits[14:12] = funct3, bits[11:7] = rd, bits[6:0] = opcode

I-type (Immediate): bits[31:20] = imm[11:0], bits[19:15]

= rs1, bits[14:12] = funct3, bits[11:7] = rd, bits[6:0] = opcode **S-type (Store):** bits[31:25] = imm[11:5], bits[24:20] = rs2, bits[19:15] = rs1, bits[14:12] = funct3, bits[11:7] = imm[4:0],

bits[6:0] = opcode

B-type (Branch): bits[31] = imm[12], bits[30:25] = imm[10:5], bits[24:20] = rs2, bits[19:15] = rs1, bits[14:12]

= funct3, bits[11:8] = imm[4:1], bits[7] = imm[11], bits[6:0]

= opcode

U-type (Upper Immediate): bits[31:12] = imm[31:12], bits[11:7] = rd, bits[6:0] = opcode

J-type (Jump): bits[31] = imm[20], bits[30:21] = imm[10:1], bits[20] = imm[11], bits[19:12] = imm[19:12], bits[11:7] = rd, bits[6:0] = opcode

- **ALU**: Arithmetic Logic Unit
- **API**: Application Programming Interface
- **ASIL**: Automotive Safety Integrity Level
- **BOM**: Bill of Materials
- **BOOM**: Berkeley Out-of-Order Machine
- **CAGR**: Compound Annual Growth Rate
- **CISC**: Complex Instruction Set Computer
- **CSR**: Control and Status Register
- **CVA6**: CERN Verilog Architecture 6 (Ariane)
- **DSP**: Digital Signal Processing
- **ECU**: Engine Control Unit
- **EH**: Embedded High-Performance (WD SweRV)
- **EL**: Embedded Low-Power (WD SweRV)
- **FDSOI**: Fully-Depleted Silicon-On-Insulator
- **FPU**: Floating-Point Unit
- **FP64**: Double-Precision Floating-Point
- **FP32**: Single-Precision Floating-Point
- **GHz**: Gigahertz
- **GMACS**: Giga Multiply-Accumulate Operations Per Second
- **GP**: General-Purpose

- **HDL**: Hardware Description Language
- **HPC**: High-Performance Computing
- **I2C**: Inter-Integrated Circuit
- **ISA**: Instruction Set Architecture
- **IoT**: Internet of Things
- **L1**: Level 1 cache
- **L2**: Level 2 cache
- **L3**: Level 3 cache
- **LPDDR**: Low-Power Double Data Rate
- **MHz**: Megahertz
- **MIPS**: Million Instructions Per Second
- **MMU**: Memory Management Unit
- **M-mode**: Machine Mode (RISC-V)
- **ML**: Machine Learning
- **NMOS**: N-Channel Metal-Oxide-Semiconductor
- **OoO**: Out-of-Order
- **OTA**: Over-The-Air
- **PC**: Program Counter
- **PLC**: Programmable Logic Controller
- **RV32E**: RISC-V 32-bit Embedded (16 registers)
- **RV32I**: RISC-V 32-bit Base Integer
- **RV64I**: RISC-V 64-bit Base Integer
- **RV128I**: RISC-V 128-bit Base Integer
- **RISC**: Reduced Instruction Set Computer
- **RTOS**: Real-Time Operating System
- **S-mode**: Supervisor Mode (RISC-V)
- **SIMD**: Single Instruction Multiple Data
- **SoC**: System-on-Chip
- **SPUR**: Symbolic Processing Using RISC
- **SPI**: Serial Peripheral Interface
- **SRAM**: Static Random-Access Memory
- **SweRV**: Western Digital open-source core
- **TEE**: Trusted Execution Environment
- **TFlops**: Tera Floating-Point Operations Per Second
- **TFLOPS**: Trillion Floating-Point Operations Per Second
- **TLB**: Translation Lookaside Buffer

- **TOPS**: Tera Operations Per Second
- **UART**: Universal Asynchronous Receiver/Transmitter
- **U-mode**: User Mode (RISC-V)
- **VLSI**: Very-Large-Scale Integration
- **WD**: Western Digital
- **X extension**: Custom/eXperimental extension (RISC-V)
- **Z extension**: Reserved extension space (RISC-V)